# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications

# 74HC/HCT74
# Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

# Dual D-type flip-flop with set and reset; positive-edge trigger

# 74HC/HCT74

## FEATURES

- Output capability: standard
- $I_{CC}$ category: flip-flops

## GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay | $C_L$ = 15 pF; $V_{CC}$ = 5 V | | | |
| | nCP to nQ, n$\overline{Q}$ | | 14 | 15 | ns |
| | n$\overline{S}_D$ to nQ, n$\overline{Q}$ | | 15 | 18 | ns |
| | n$\overline{R}_D$ to nQ, n$\overline{Q}$ | | 16 | 18 | ns |
| $f_{max}$ | maximum clock frequency | | 76 | 59 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per flip-flop | notes 1 and 2 | 24 | 29 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V
2. For HC the condition is $V_I$ = GND to $V_{CC}$

   For HCT the condition is $V_I$ = GND to $V_{CC}$ − 1.5 V

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| 74HC(T)74N | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| 74HC(T)74D | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HCT74DB | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74HCT74PW | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 13 | $1\overline{R}_D$, $2\overline{R}_D$ | asynchronous reset-direct input (active LOW) |
| 2, 12 | 1D, 2D | data inputs |
| 3, 11 | 1CP, 2CP | clock input (LOW-to-HIGH, edge-triggered) |
| 4, 10 | $1\overline{S}_D$, $2\overline{S}_D$ | asynchronous set-direct input (active LOW) |
| 5, 9 | 1Q, 2Q | true flip-flop outputs |
| 6, 8 | $1\overline{Q}$, $2\overline{Q}$ | complement flip-flop outputs |
| 7 | GND | ground (0 V) |
| 14 | $V_{CC}$ | positive supply voltage |

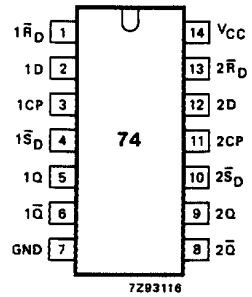



Fig.1 Pin configuration.

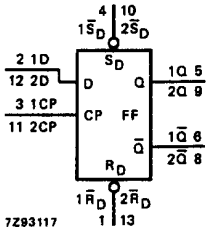



Fig.2 Logic symbol.

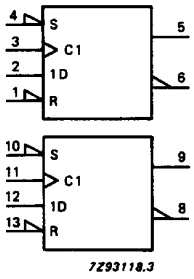



Fig.3 IEC logic symbol.

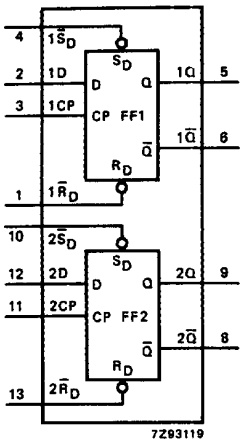



Fig.4 Functional diagram.

**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{S}_D$ | $\overline{R}_D$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{S}_D$ | $\overline{R}_D$ | CP | D | $Q_{n+1}$ | $\overline{Q}_{n+1}$ |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

**Note**

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH CP transition
   $Q_{n+1}$ = state after the next LOW-to-HIGH CP transition

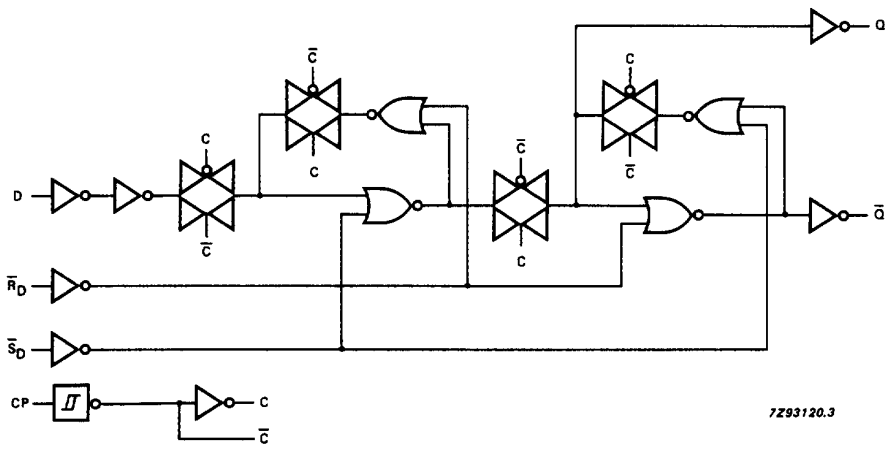



Fig.5 Logic diagram (one flip-flop).

### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: flip-flops

### AC CHARACTERISTICS

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | $V_{CC}$ (V) | WAVEFORMS |
| | | min. | typ. | max. | min. | max | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay nCP to nQ, n$\overline{Q}$ | | 47 | 175 | | 220 | | 265 | ns | 2.0 | Fig.6 |
| | | | 17 | 35 | | 44 | | 53 | | 4.5 | |
| | | | 14 | 30 | | 37 | | 45 | | 6.0 | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$ | | 50 | 200 | | 250 | | 300 | ns | 2.0 | Fig.7 |
| | | | 18 | 40 | | 50 | | 60 | | 4.5 | |
| | | | 14 | 34 | | 43 | | 51 | | 6.0 | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$ | | 52 | 200 | | 250 | | 300 | ns | 2.0 | Fig.7 |
| | | | 19 | 40 | | 50 | | 60 | | 4.5 | |
| | | | 15 | 34 | | 43 | | 51 | | 6.0 | |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 19 | 75 | | 95 | | 110 | ns | 2.0 | Fig.6 |
| | | | 7 | 15 | | 19 | | 22 | | 4.5 | |
| | | | 6 | 13 | | 16 | | 19 | | 6.0 | |
| $t_W$ | clock pulse width HIGH or LOW | 80 | 19 | | 100 | | 120 | | ns | 2.0 | Fig.6 |
| | | 16 | 7 | | 20 | | 24 | | | 4.5 | |
| | | 14 | 6 | | 17 | | 20 | | | 6.0 | |
| $t_W$ | set or reset pulse width LOW | 80 | 19 | | 100 | | 120 | | ns | 2.0 | Fig.7 |
| | | 16 | 7 | | 20 | | 24 | | | 4.5 | |
| | | 14 | 6 | | 17 | | 20 | | | 6.0 | |
| $t_{rem}$ | removal time set or reset | 30 | 3 | | 40 | | 45 | | ns | 2.0 | Fig.7 |
| | | 6 | 1 | | 8 | | 9 | | | 4.5 | |
| | | 5 | 1 | | 7 | | 8 | | | 6.0 | |
| $t_{su}$ | set-up time nD to nCP | 60 | 6 | | 75 | | 90 | | ns | 2.0 | Fig.6 |
| | | 12 | 2 | | 15 | | 18 | | | 4.5 | |
| | | 10 | 2 | | 13 | | 15 | | | 6.0 | |
| $t_h$ | hold time nCP to nD | 3 | −6 | | 3 | | 3 | | ns | 2.0 | Fig.6 |
| | | 3 | −2 | | 3 | | 3 | | | 4.5 | |
| | | 3 | −2 | | 3 | | 3 | | | 6.0 | |
| $f_{max}$ | maximum clock pulse frequency | 6.0 | 23 | | 4.8 | | 4.0 | | MHz | 2.0 | Fig.6 |
| | | 30 | 69 | | 24 | | 20 | | | 4.5 | |
| | | 35 | 82 | | 28 | | 24 | | | 6.0 | |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: flip-flops

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

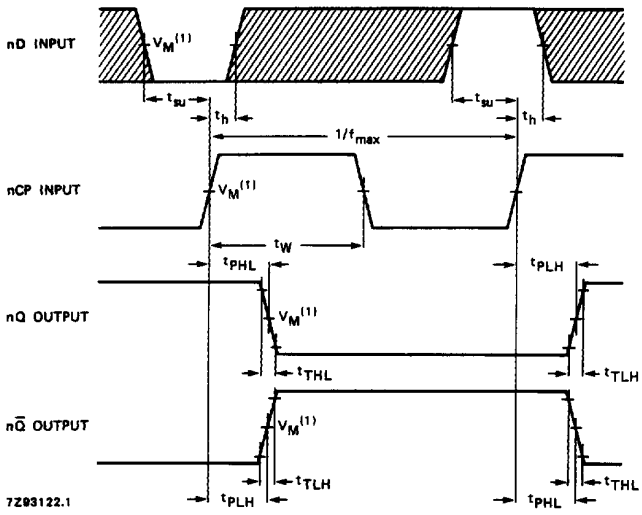
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| nD | 0.70 |
| $n\overline{R}_D$ | 0.70 |
| $n\overline{S}_D$ | 0.80 |
| nCP | 0.80 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay nCP to nQ, $n\overline{Q}$ | | 18 | 35 | | 44 | | 53 | ns | 4.5 | Fig.6 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$ | | 23 | 40 | | 50 | | 60 | ns | 4.5 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$ | | 24 | 40 | | 50 | | 60 | ns | 4.5 | Fig.7 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |
| $t_W$ | clock pulse width HIGH or LOW | 18 | 9 | | 23 | | 27 | | ns | 4.5 | Fig.6 |
| $t_W$ | set or reset pulse width LOW | 16 | 9 | | 20 | | 24 | | ns | 4.5 | Fig.7 |
| $t_{rem}$ | removal time set or reset | 6 | 1 | | 8 | | 9 | | ns | 4.5 | Fig.7 |
| $t_{su}$ | set-up time nD to nCP | 12 | 5 | | 15 | | 18 | | ns | 4.5 | Fig.6 |
| $t_h$ | hold time nCP to nD | 3 | −3 | | 3 | | 3 | | ns | 4.5 | Fig.6 |
| $f_{max}$ | maximum clock pulse frequency | 27 | 54 | | 22 | | 18 | | MHz | 4.5 | Fig.6 |

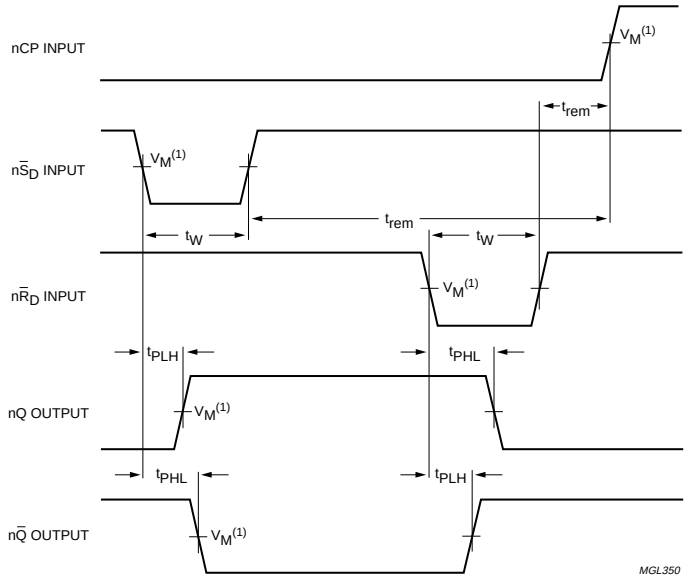
## AC WAVEFORMS




The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

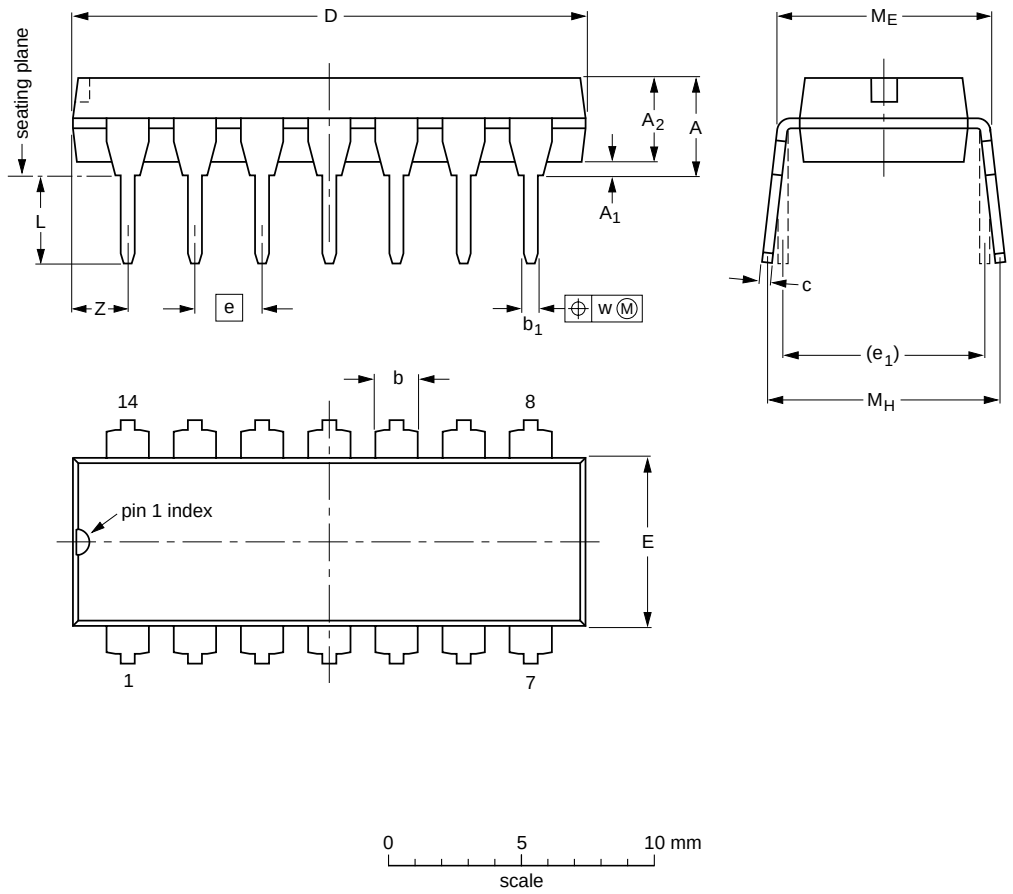



(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the set ($nS_D$) and reset ($nR_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the $nR_D$, $nS_D$ to nCP removal time.

## PACKAGE OUTLINES

**DIP14: plastic dual in-line package; 14 leads (300 mil)** **SOT27-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

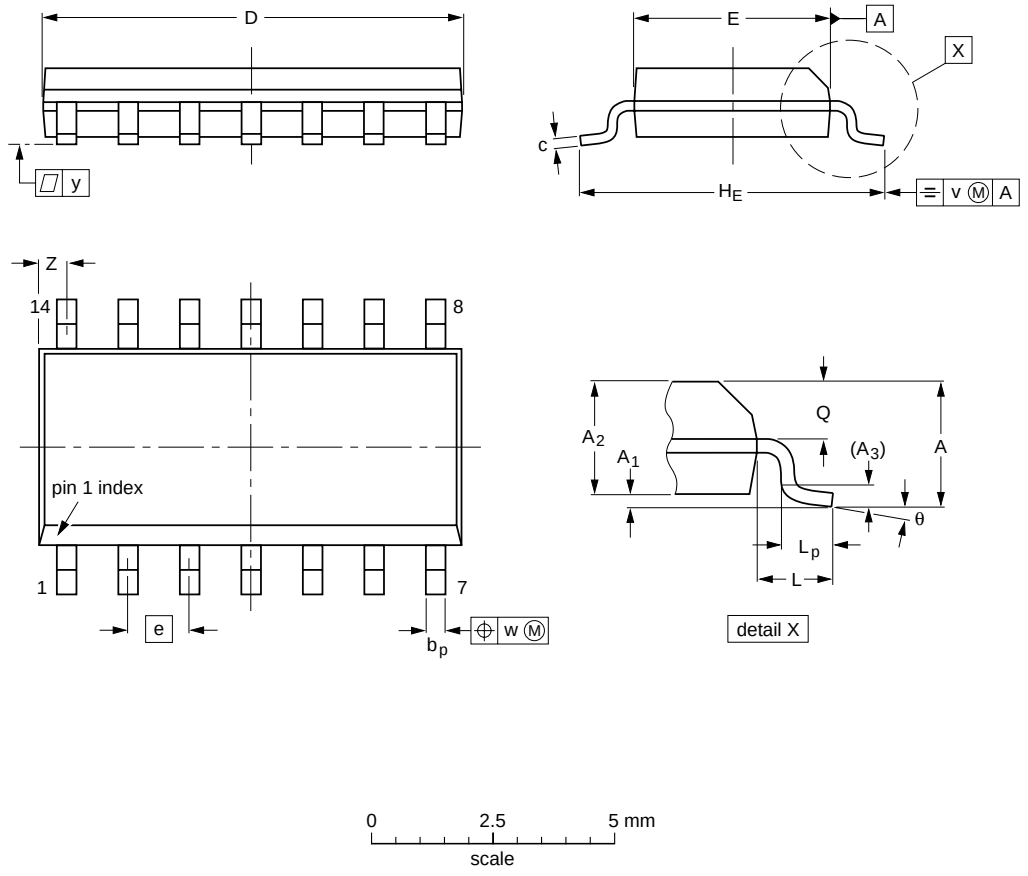
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.13 | 0.53<br>0.38 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 2.2 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.087 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT27-1 | 050G04 | MO-001AA | | | | ~~92-11-17~~<br>95-03-11 |

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

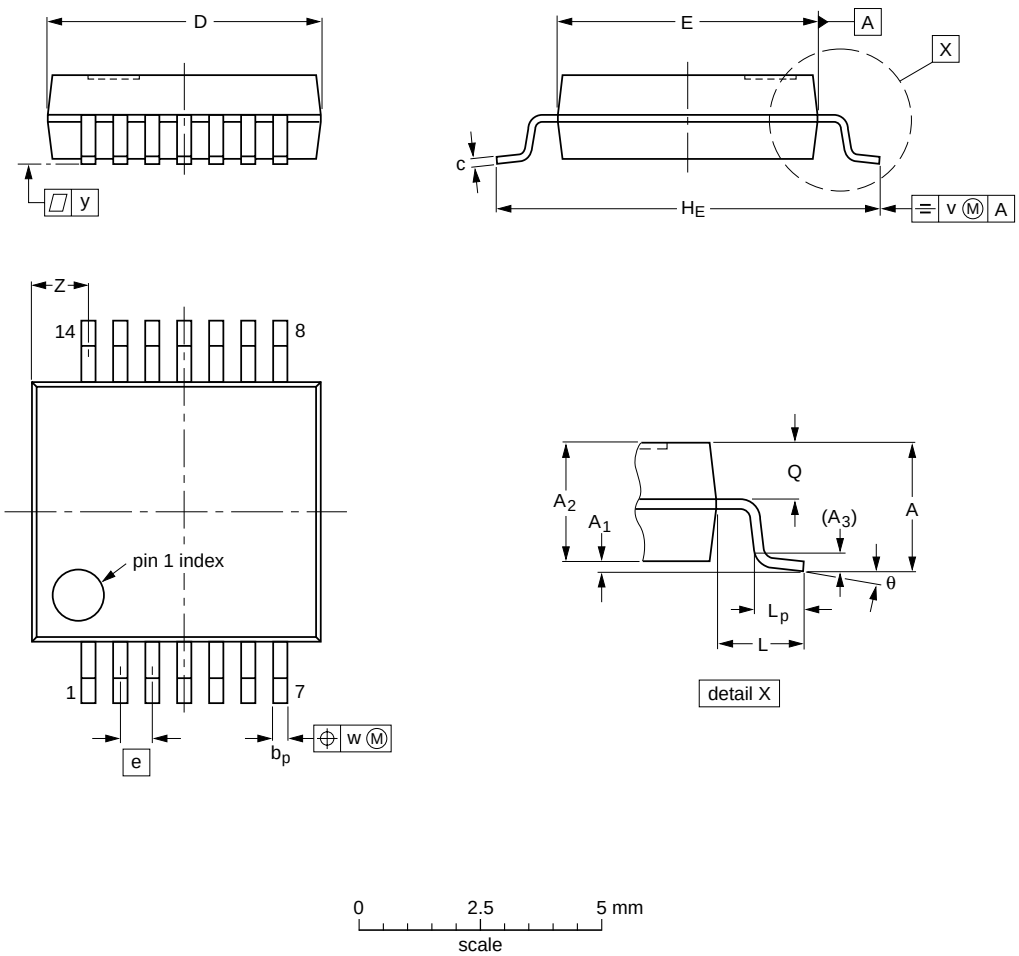
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT108-1 | 076E06S | MS-012AB | | | | ~~95-01-23~~<br>97-05-22 |

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm** **SOT337-1**




**DIMENSIONS (mm are the original dimensions)**

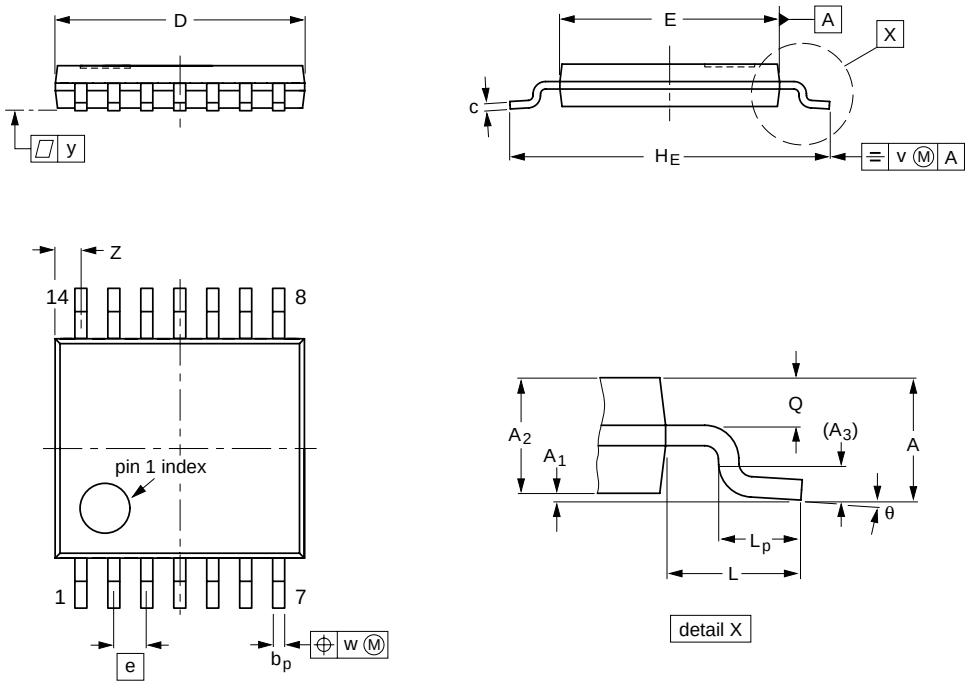
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT337-1 | | MO-150AB | | | | ~~95-02-04~~<br>96-01-18 |

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT402-1 | | MO-153 | | | | ~~94-07-12~~<br>95-04-04 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

**Even with these conditions:**

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.