Order Number: MC13180TB/D
Rev. 0, 12/2001

Preliminary
Technical Brief

2.4 GHz Low Power Wireless Data Transceiver for Bluetooth™ Applications

MC13180

The MC13180 2.4 GHz Low Power Wireless Data Transceiver for Bluetooth is a part of the comprehensive Bluetooth platform from Motorola that provides a complete, low–power Bluetooth Radio System for Bluetooth Class 1 or 2 power systems. The design is based on Motorola's third–generation Bluetooth architecture that has set the industry standard for interoperability, complete functionality, and compliance with the Bluetooth specification. When combined with a specified Motorola baseband controller such as the MC71000, a complete Bluetooth solution can be realized.

The MC13180 provides a unique combination of sensitivity, excellent C/I performance, and low power consumption. These performance parameters are extremely important to maintaining a robust link in high RF interference environments like mobile phones, high density Bluetooth networks, 802.11b networks, microwave ovens, etc.

- Power Supply Range: 2.5 to 3.1 V
- Low Current Drain in Transmit (29 mA Peak) or Receive (37 mA Peak) Mode
- Power Down Modes for Power Conservation
- Minimum External Components
- Low IF Receiver with On–Chip Filters
- Fully Integrated Demodulator with A/D
- Direct Launch Transmitter
- Multi–Accumulator, Dual–Port, Fractional–N Synthesizer
- RSSI with A/D
- Crystal Independent (12 to 15 MHz) Reference Oscillator or 12 to 20 MHz if supplied externally

Package Information

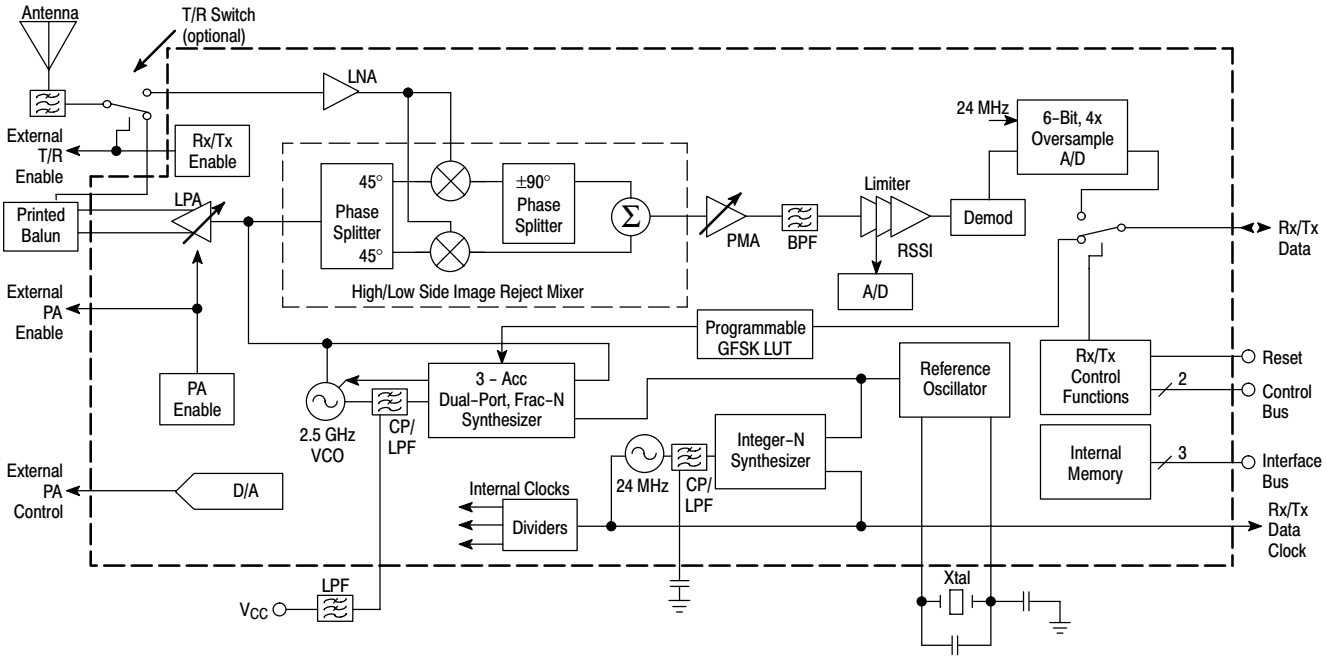
Plastic Package
Case 1314
(QFN–48)

Ordering Information

Device	Operating Temperature Range	Package
MC13180	T_A = –20 to 85°C	QFN–48

1 Block Diagram

Figure 1. Simplified Block Diagram



Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage $V_{CC}RF$ V_{DDINT}		 3.2 3.2	V
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–60 to 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Contact Descriptions section.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	$V_{CC}RF$	2.5	2.7	3.1	Vdc
Power Supply Voltage, Logic Interface ($V_{DDINT} \leq V_{CC}RF$)	V_{DDINT}	1.65	–	$V_{CC}RF$	Vdc
Input Frequency	f_{in}	2.4	–	2.5	GHz
Ambient Temperature Range	T_A	–20	25	85	°C
Ref Osc Freqency Range (only integral multiples of 20 kHz may be used) With Crystal External Source	f_{ref}	 12 12	 13 –	 15 20	MHz

Digital DC Electrical Specifications ($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Current $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN, V_{in} = 0 V or 2.5 V	I_{CCINT}	–	2.0	–	µA
Radio Power Supply Current, Sleep Mode	$I_{CCRFsleep}$	–	2.0	–	µA
Radio Power Supply Current					mA
Transmit, 1 Slot	$I_{CCRFtx1}$	–	23	–	
Transmit, 3 Slot	$I_{CCRFtx3}$	–	27	–	
Transmit, 5 Slot	$I_{CCRFtx5}$	–	28	–	
Transmit, Continuous	$I_{CCRFtxc}$	–	29	–	
Radio Power Supply Current					mA
Receive, 1 Slot	$I_{CCRFrx1}$	–	30	–	
Receive, 3 Slot	$I_{CCRFrx3}$	–	34	–	
Receive, 5 Slot	$I_{CCRFrx5}$	–	35	–	
Receive, Continuous	$I_{CCRFrxc}$	–	37	–	
Output Voltage Low SDATA, CLK, FS, RFDATA	V_{OL}				mV
ILoad = 0 µA		–	20	–	
ILoad = 100 µA		–	TBD	–	
Output Voltage High SDATA, CLK, FS, RFDATA	V_{OH}				V
ILoad = 0 µA		–	2.48	–	
ILoad = 100 µA		–	TBD	–	
Output Voltage Low EPAEN, GPO	V_{OL}				mV
ILoad = 0 µA		–	20	–	
ILoad = 100 µA		–	TBD	–	
Output Voltage High EPAEN, GPO	V_{OH}				V
ILoad = 0 µA		–	2.68	–	
ILoad = 100 µA		–	TBD	–	
Input Voltage Low $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN	V_{IL}	–	0	–	V
Input Voltage High $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN	V_{IH}	–	V_{DDINT}	–	V
Input Current $\overline{RES}$, $\overline{CE}$, SDATA, SCK, RFDATA, RTXEN, V_{in} = 0 V or 2.5 V	I_{in}	–	±1.0	–	µA

EPA DAC Electrical Specifications (V_{CCRF} = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4 except R11/7 = 1, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage EPADAC, ILoad = ±100 µA	V_{out}				V
PADAC = 000000		–	0.02	–	
PADAC = 100000		–	1.60	–	
PADAC = 111111		–	2.68	–	
Resolution	RESOL	–	6	–	Bits
Linearity	INL	–	±1.0	–	LSB
Supply Current	I_{CCDAC}	–	300	–	µA

Digital AC Electrical Specifications ($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults in Figure 4, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay, RTXEN to FS, receive mode	T_{prop}	–	172	–	µS
Strobe Delay, RTXEN to RFDATA, transmit mode	T_{stb}	–	Tx Sync Delay + 0.5	–	µS
Hold Time, RTXEN to RFDATA, transmit mode	T_{hold}	–	4.0	–	µS
Transmit Latency, RTXEN to PAout, transmit mode	T_XLAT	–	Tx Sync Delay + 2.5	–	µS
Tx Sync Delay	TXsync	172	–	192	µS
CLK Duty Cycle	TDuty	30	40/60	70	%

Receiver AC Electrical Specifications ($V_{CC}RF$ = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, Desired RF_{in} = 2.441 GHz @ f_{dev} = 160 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating data for desired signal = PRBS9, Modulating data for interferring signal = PRBS15, Measured BER < 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, unless otherwise noted. Measurements made from LNAin to Recovered Data out. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specification	Unit
Receiver Sensitivity	$SENS_{min}$					dBm
T_A = 25°C		–	–84			
T_A = –20 to 85°C		–	–78	–75	≤ –70	
Receiver Sensitivity degradation in the presence of a dirty transmitter		–	–3.0	–		dB
Maximum Usable Signal Level	$SENS_{max}$	–	–14	–	≥ –20	dBm
Co–Channel Interference @ –60 dBm	C/I co	–	7.5	–	≤ 11	dB
Adjacent Interference						dB
Adjacent (±1 MHz) Interference @ –60 dBm	C/I 1MHz	–	–8.0	–	≤ 0	
Adjacent (±2 MHz) Interference @ –60 dBm	C/I 2MHz	–	–37	–	≤ –30	
Adjacent (≥3 MHz) Interference @ –67 dBm	C/I ≥3MHz	–	–46	–	≤ –40	
Image Frequency Interference @ –67 dBm	C/I image	–	–17	–	≤ – 9.0	dB
Adjacent Interference to In–Band Image Frequency @ –67 dBm	C/I image ±1	–	–33	–	≤ –20	dB
Spurious Response Frequencies		–	2	–	5	
Intermodulation Performance [Note 1]		–	–32	–	≥ –39	dBm
Receiver Spurious Emissions						dBm
30 MHz to 1.0 GHz		–	–72	–	≤ –57	
1.0 GHz to 12.75 GHz		–	–74	–	≤ –47	
Receiver Blocking Performance						dBm
30 MHz to 2.0 GHz (1.999 GHz)		–	–16	–	≥ –10	
2.0 to 2.4 GHz (2.001 GHz)		–	–16	–	≥ –27	
2.4 to 3.0 GHz (2.401 GHz)		–	–16	–	≥ –27	
3.0 to 12.75 GHz (3.001 GHz)		–	–3.0	–	≥ –10	
RSSI Conversion Value, (R4/6 and R9/8 = 1)	RSSI					dBm
RF level at LNA input to maintain conversion value of:						
0000 (binary)		–	–40	–		
1000		–	–55	–		
1111		–	–70	–		

NOTE: 1. Measured at $f_2 - f_1$ = 5.0 MHz in accordance to Bluetooth specification.

Receiver AC Electrical Specifications (continued) (V_{CC}RF = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, Desired RF_{in} = 2.441 GHz @ f_{dev} = 160 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating data for desired signal = PRBS9, Modulating data for interferring signal = PRBS15, Measured BER < 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, unless otherwise noted. Measurements made from LNAin to Recovered Data out. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specification	Unit
RSSI Resolution (R4/6 and R9/8 = 1)	$RSSI_{res}$	–	2.0	–		dB/bit
RSSI Supply Current (R4/6 and R9/8 = 1)		–	60	–		μA

NOTE: 1. Measured at $f_2 - f_1$ = 5.0 MHz in accordance to Bluetooth specification.

Transmitter AC Electrical Specifications (V_{CC}RF = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Reference Crystal = 13 MHz, Register bit settings according to Figure 4, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specification	Unit
RF Transmit Output Power	P_{out}					dBm
T_A = 25°C		–	2.0	–		
T_A = 85°C		–	0	–		
T_A = –20°C		–	3.0	–	–6.0 to 4.0	
–20 dBc Occupied Bandwidth	OccBW	–	930	–	≤1000	kHz
In–Band Spurious Emissions						dBm
Adjacent Channel ±2.0 MHz Offset	Inb2	–	–59	–	≤ –20	
Adjacent Channel ±3.0 MHz Offset	Inb3	–	–65	–	≤ –40	
Adjacent Channel ≥3.0 MHz Offset	Inbg3	–	–70	–	≤ –40	
In Band Spurious Emission Exceptions	Inbex	–	0	–	≤ 3	
Out of Band Spurious Emissions						dBm
30 MHz to 1.0 GHz	Outb1	–	–57	–	≤ –36	
1.0 to 12.75 GHz (2nd Harmonic)	Outb2	–	–25	–	≤ –30	
1.8 to 1.9 GHz	Outb3	–	–58	–	≤ –47	
5.15 to 5.3 GHz	Outb4	–	–56	–	≤ –47	
Peak Frequency Deviation	Dev	–	157.5	–	140 to 175	kHz
Minimum Frequency Deviation	DevMin	–	138	–	115	kHz
High vs Low Frequency Modulation Percentage	ModIn	–	86	–	≥ 80	%
Initial Frequency Accuracy	InitFA	–	±5.0	–	±75	kHz
Transmitter Center Frequency Drift						kHz
One–slot packet	d1	–	±5.5	–	±25	
Three–slot packet	d3	–	±6.5	–	±40	
Five–slot packet	d5	–	±7.7	–	±40	
Maximum Frequency Drift	Dmax	–	4.3	–	20	kHz/ 50 μS

Receiver AC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Maximum Usable Signal Level, T_A = –20 to 85°C	SENSmax	–	≥ –20	–	dBm
Receiver Blocking Performance, T_A = 25°C					dBm
W–CDMA 1.8 GHz		–	–16	–	
W–CDMA 2.2 GHz		–	–16	–	
GSM 1.8 GHz		–	–16	–	
Co–Channel Interference @ –60 dBm, T_A = –20 to 85°C	C/I co	–	7.5	–	dB
Adjacent Interference, T_A = 25°C					dB
Adjacent (±1 MHz) Interference @ –70 dBm	C/I 1MHz	–	–8.0	–	
Adjacent (±2 MHz) Interference @ –70 dBm	C/I 2MHz	–	–41	–	
Adjacent (≥3 MHz) Interference @ –77 dBm	C/I ≥3MHz	–	–47	–	
Image Frequency Interference @ –77 dBm, T_A = 25°C	C/I image	–	–17	–	dB
Adjacent Interference to In–Band Image Frequency @ –77 dBm, T_A = 25°C	C/I image ±1	–	–33	–	dB
LNA Input Impedance					dB
LNA Enabled	$S11_{en}$	–	–8.5 ∠ –122	–	
LNA Disabled	$S11_{dis}$	–	–4.6 ∠ 27	–	

Reference Oscillator Electrical Characteristics (V_{CC}RF = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, T_A = 25°C, Reference Crystal = 13 MHz, Register bit settings according to specified defaults, unless otherwise noted. See Figure 3 Test Circuit.)

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal Frequency Range		12	–	15	MHz
External Driver Frequency Range		12	–	20	MHz
Crystal Load Capacitance		–	13	–	pF
Trim Capacitance Range		–	0 to 9.3	–	pF
Trim Capacitance Resolution		–	0.3	–	pF

SPI AC Electrical Characteristics (V_{CC}RF = 2.7 Vdc, V_{DDINT} = 2.5 Vdc, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
$\overline{CE}$ to SCK					nS
Setup Time	T_{su}	–	TBD	–	
Hold Time	T_{hold}	–	TBD	–	
SDATA to SCK					nS
Setup Time	T_{su}	–	TBD	–	
Hold Time	T_{hold}	–	TBD	–	
SCK to SDATA Propagation Delay	T_{prop}	–	TBD	–	nS
SCK Operating Frequency (50% Duty Cycle)	f_{max}	–	25	–	MHz

2 Contact Connections

Figure 2. Device Pinout

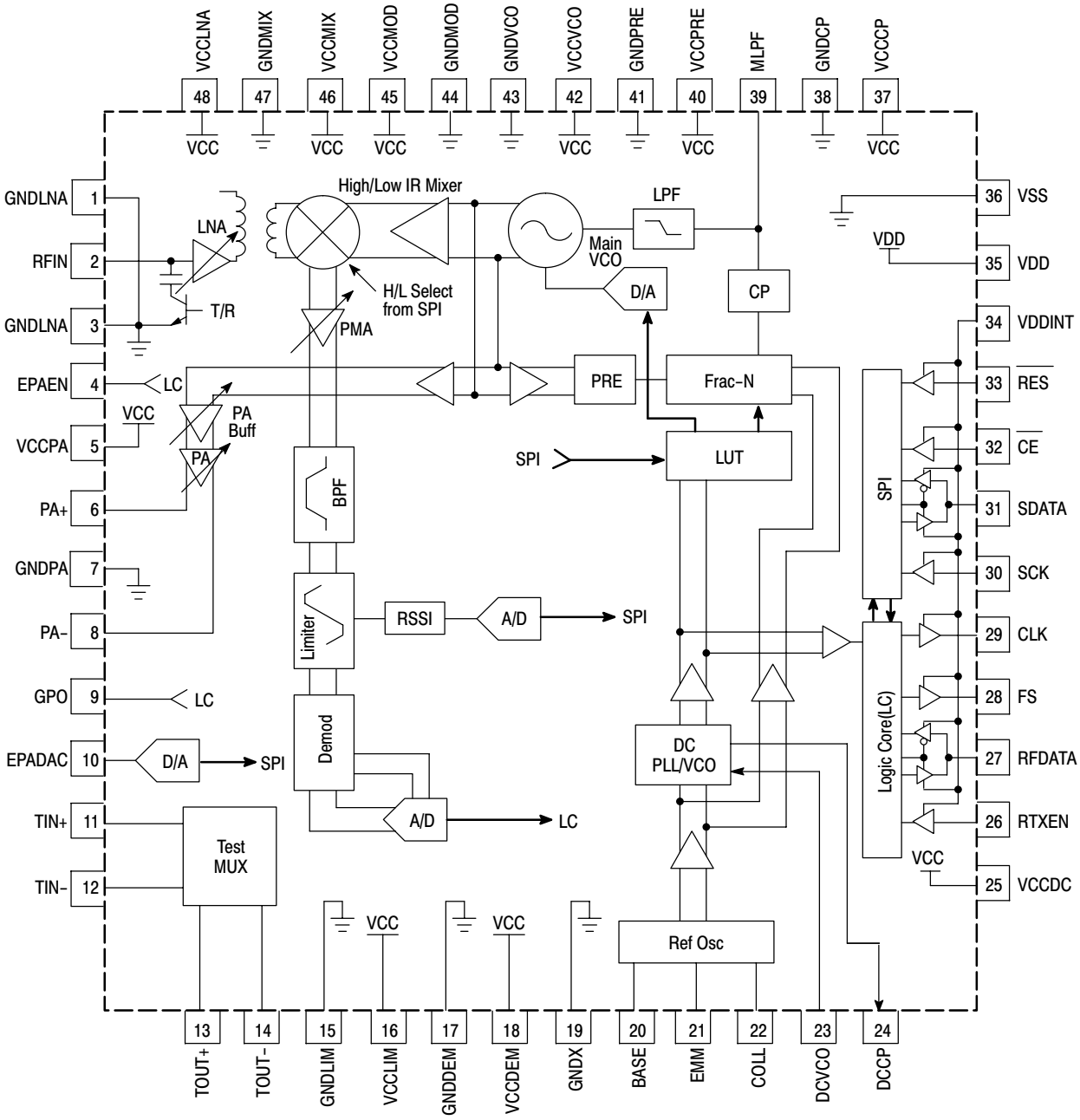


Figure 3. Test Circuit

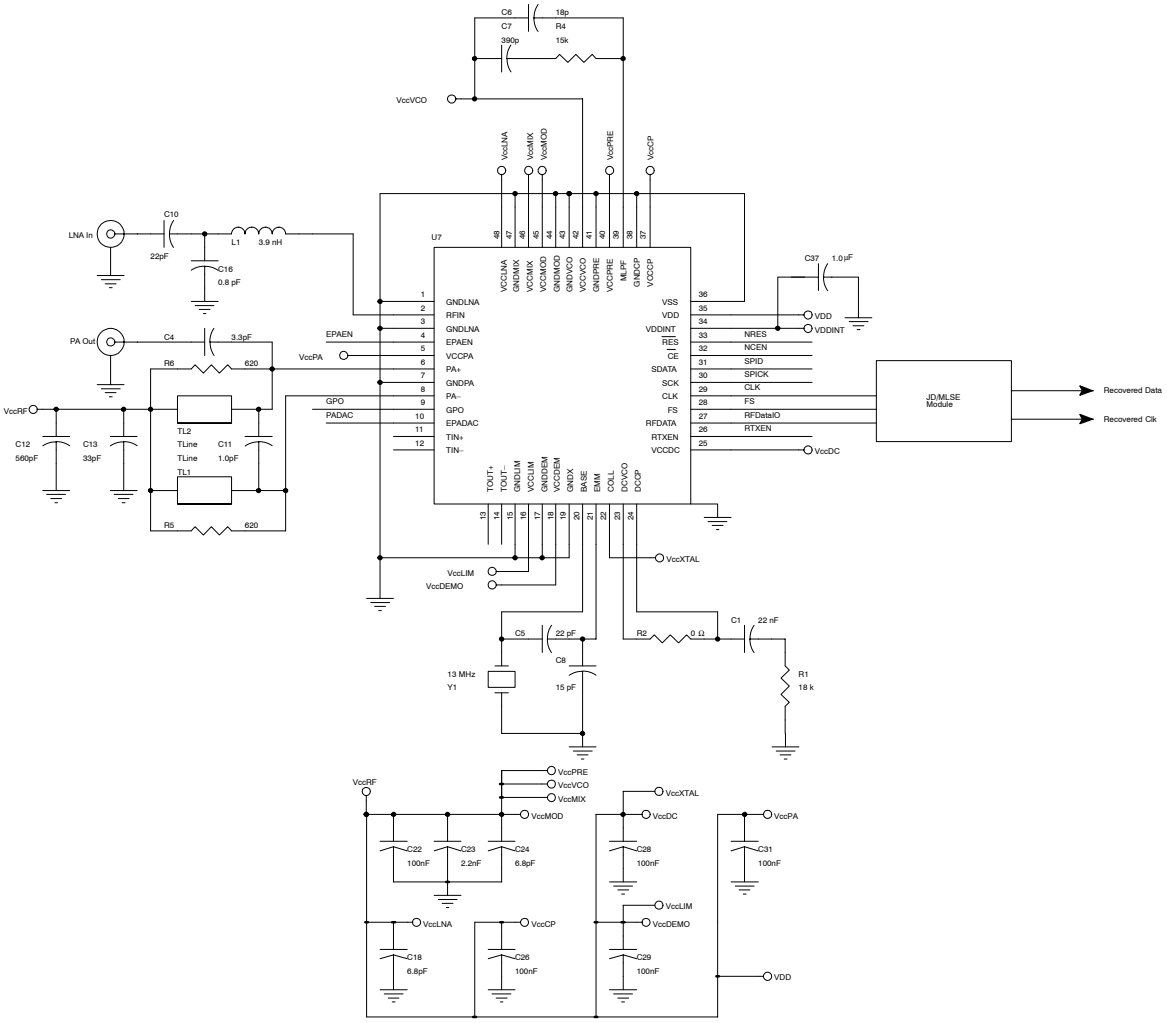


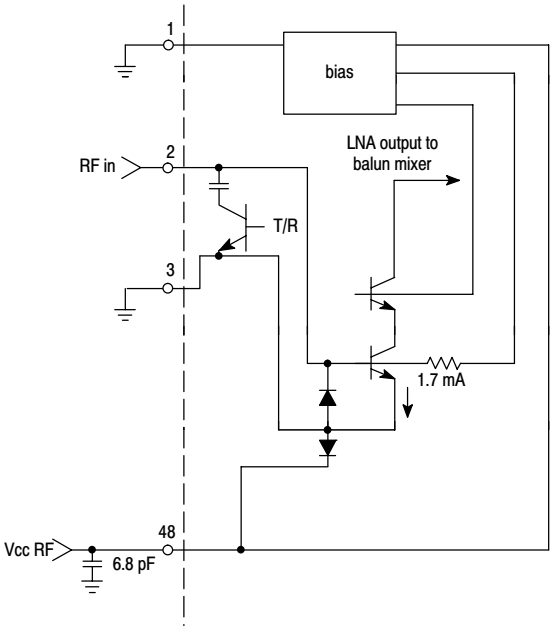
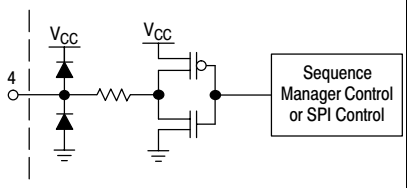
Figure 4. Register Map

MC13180:		Byte 1								Byte 0							
Register Address	Register Number	MSB Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
$00 Programmable Reset																	
$01	1	MSB 16 Bit Frac–N Numerator Divide Value – num LSB															
	Rx Test	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	0
	Tx Test	1	1	0	0	0	0	1	1	1	1	0	1	0	0	1	0
$02	2	Sleep Enable	Tx Enable	Rx Enable		High/Low Injection Enable				MSB Frac–N Integer Divide Value LSB							
	Rx Test	0	0	1	0	1	0	0	0	1	0	1	1	1	0	0	1
	Tx Test	0	1	0	0	0	0	0	0	1	0	1	1	1	0	0	0
$03	3						General Purpose Output Programmable Delay			General Purpose Output Select	General Purpose Output	MSB PA DAC Setting LSB					
		1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
$04	4	LNA Gain Adjust		PMA Gain Adjust		External PA Turned On First			RSSI Read Delay		RSSI Read Enable						
		1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1
$05	5											PA Buffer Bias Adjust					
		0	1	1	0	1	1	1	0	1	1	0	1	1	1	0	0
$06	6	EPAEN = not(GPO)	MSB Xtal Trim				LSB	MSB DC PII R Counter LSB									
		0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0
$07	7		Extend Dual Port Delay Range	Dual Port Programmable Delay For Tx PLL			MSB	DC PII N Counter LSB									
		0	1	1	0	1	1	0	0	1	0	1	1	0	0	0	0
$08	8	MSB Transmit Synchronization Time Delay Value LSB								MSB Dual Port Digital Multiplier Value For Tx PLL LSB							
		1	0	1	0	1	1	0	0	1	0	0	0	0	1	1	1
$09	9								RSSI Enable								
		0	0	1	1	1	1	1	0	1	1	0	1	1	1	1	1
$0A	10																
		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$0B	11									External PA DAC Enable	External PA Enable		Xtal Boost Enable	Xtal Buffer Output Current Enable	Xtal Buffer Enable	Xtal Bias Enable	Xtal Enable
		1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1
$0C	12	MSB ROM_r2_c2 LSB								MSB ROM_r1_c1 LSB							
		1	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
$0D	13	MSB ROM_r2_c4 LSB								MSB ROM_r2_c3 LSB							
		1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	1
$0E	14	MSB ROM_r3_c2 LSB								MSB ROM_r3_c1 LSB							
		0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1
$0F	15	MSB ROM_r3_c4 LSB								MSB ROM_r3_c3 LSB							
		1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	0
$10	16	MSB ROM_r4_c3 LSB								MSB ROM_r4_c2 LSB							
		1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	0
$11	17									MSB ROM_r4_c4 LSB							
		0	0	0	0	1	1	1	1	1	0	1	0	1	1	0	1
$12	18																

Figure 4. Register Map (continued)

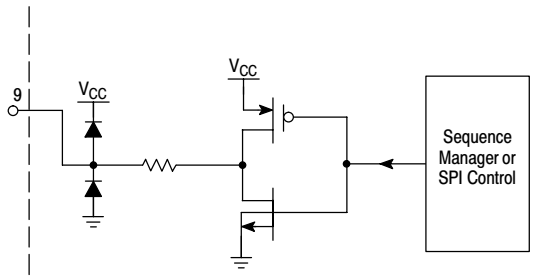
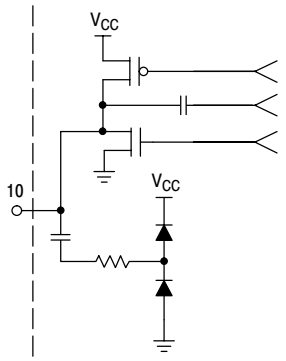
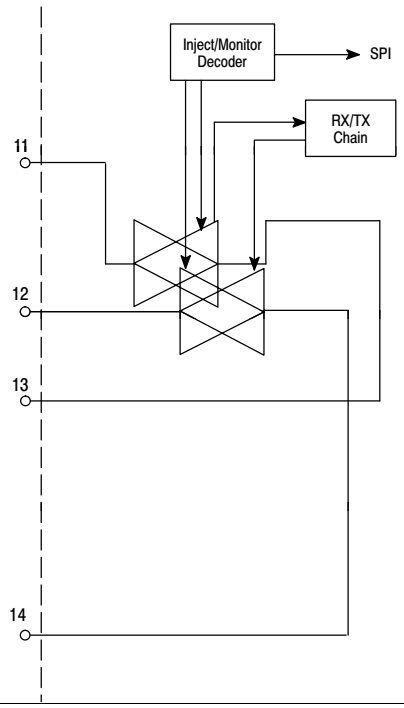
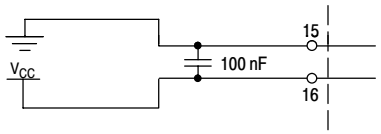
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$13	19																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$14	20																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$15	21																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$16	22																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$17	23																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$18	24																
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
$19	25																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
$1A	26																
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
$1B	27																
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1
$1C	28 Read Only																
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$1D	29 Read Only													MSB	RSSI Conversion		LSB
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$1E	30 Read Only	Bit 3:0 of Part Number			LSB	Manuf. ID (continuation code)				MSB	Manuf. ID (non–continuation code)					LSB	1
		1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
$1F	31 Read Only	MSB	Version Number		LSB	MSB	Bit 15:4 of Part Number										
		0	0	0	1	0	0	1	1	0	0	1	1	0	1	1	1

Table 1. Contact Definitions

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
1	GNDLNA		**GNDLNA, Negative supply** GNDLNA is the ground for the LNA.
2	RFIN		**RFIN** RFIN is the RF input to the LNA. The LNA is a bipolar cascode design. The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain. The cascode output drives the primary of an on–chip balun single–endedly.
3	GNDLNA		**GNDLNA, Negative supply** GNDLNA is the ground for the LNA.
48	VCCLNA		**VCCLNA, Positive supply** VCCLNA is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It is decoupled to GNDLNA at the pin of the IC.
4	EPAEN		**EPAEN** External PA enable is a digital output which can be used to enable an external PA. It can be controlled via SPI or placed under sequence manager control. This output can also be used to control an external T/R switch.
5	VCCPA	See Figure 5.	**VCCPA,** Positive Supply VCCPA pin is taken to the incoming positive battery or regulated dc voltage through a low impedance trace on the PCB. It is decoupled to GNDPA at the pin of the IC.
7	GNDPA		**GNDPA**, **Negative Supply** GNDPA pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A multi–sided PCB is implemented so that ground returns can be easily made through via holes.
6	PA+		**PA +** Positive differential PA output. An external differential–to–single–ended matching network is desired.
8	PA –		**PA –** Negative differential PA output. An external differential–to–single–ended matching network is desired.

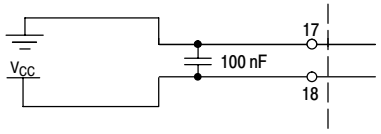
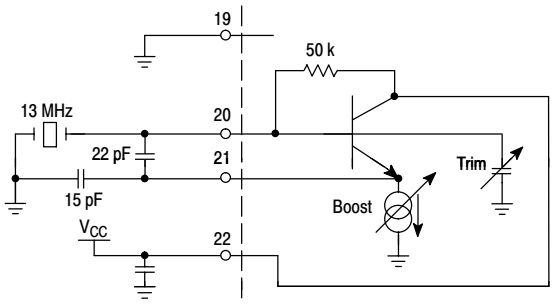
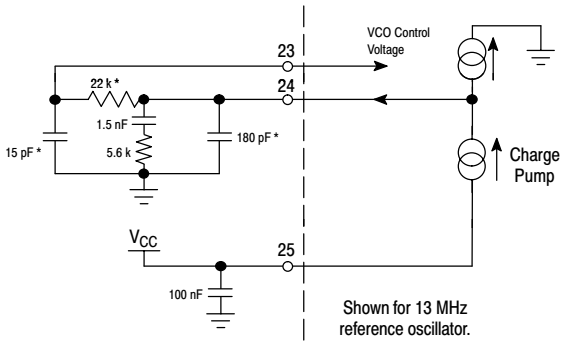
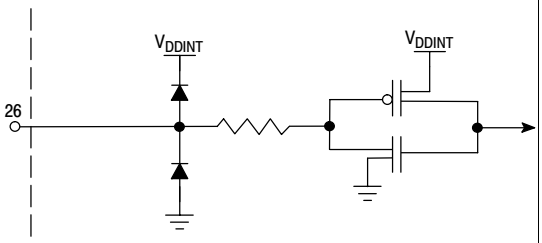
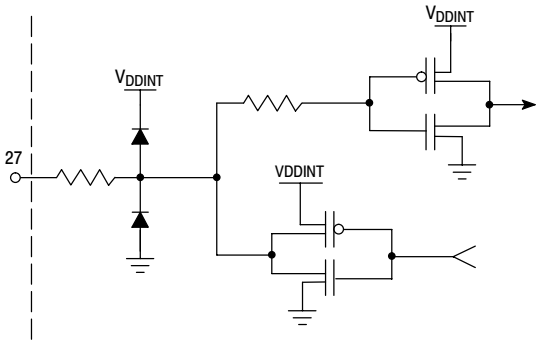
NOTE: VCC = V_{CC}RF

Table 1. Contact Definitions (continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
9	GPO		**GPO** The General Purpose Output is a digital output. GPO can be controlled by the SPI or by the Sequence Manager. This signal can also be used to control an external T/R Switch.
10	EPADAC		**EPADAC** External PA driver. Analog output ranges from 0 to V_{CC} PA.
11	TIN +		**TIN +** TIN + may be selected as a point of signal injection via programming a SPI word in order to characterize a desired block or blocks. This pin is for factory use only.
12	TIN –		**TIN –** TIN – may be selected as a point of signal injection via programming a SPI word in order to characterize a desired block or blocks. This pin is for factory use only.
13	TOUT +		**TOUT +** TOUT + may be selected as a point of signal monitoring via programming a SPI word in order to characterize a desired block or blocks. This pin is for factory use only.
14	TOUT –		**TOUT –** TOUT – may be selected as a point of signal monitoring via programming a SPI word in order to characterize a desired block or blocks. This pin is for factory use only.
15	GNDLIM		**GNDLIM, Negative supply** GNDLIM is the ground for limiter.
16	VCCLIM		**VCCLIM, Positive supply** VCCLIM is decoupled to GNDLIM at the pin of the IC.

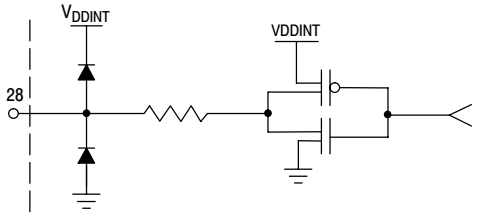
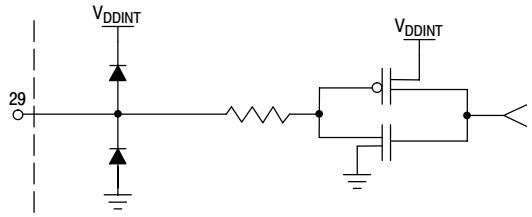
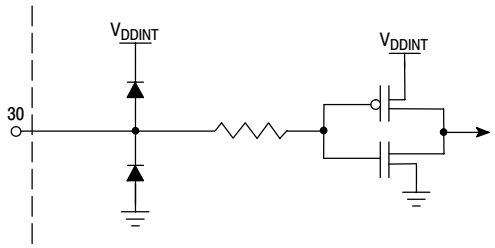
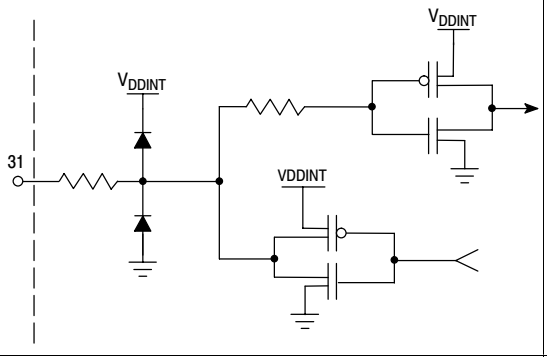
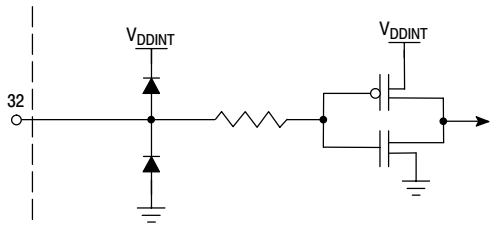
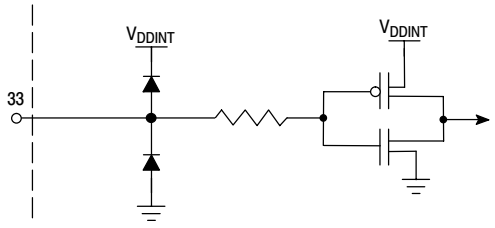
NOTE: VCC = V_{CC}RF

Table 1. Contact Definitions (continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
17	GNDDEMO		**GNDDEM, Negative supply** GNDDEM is the ground for demodulator.
18	VCCDEMO		**VCCDEM, Positive supply** VCCDEM is decoupled to GNDDEM at the pin of the IC.
19	GNDX	 Shown for 13 MHz reference oscillator.	**GNDX** Reference oscillator ground.
20	BASE		**BASE** Reference oscillator base. The base is the reference oscillator input. An on–chip capacitor trim network is also included to allow the user to use relatively inexpensive crystals.
21	EMM		**EMM** Reference oscillator emitter. A bias current of 50 μA with boost capability of 200 μA is supplied internally to the emitter.
22	COLL		**COLL** Reference oscillator collector. The collector is tied to VCC. The pin of the IC is bypassed to gnd.
23	DCVCO		**DCVCO** Data Clock Loop Filter VCO control voltage.
24	DCCP		**DCCP** Data Clock Loop Filter charge pump. *Components are optional
25	VCCDC		**VCCDC** Data clock VCC. The pin of the IC is bypassed to gnd.
26	RTXEN		**RTXEN** When RTXEN is asserted (high), it controls the start of the Rx or Tx cycle. Digital input.
27	RFDATA		**RFDATA** This digital I/O is used for Transmit Data (input) and Received Data (output).

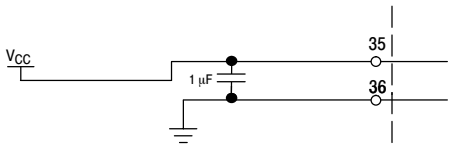
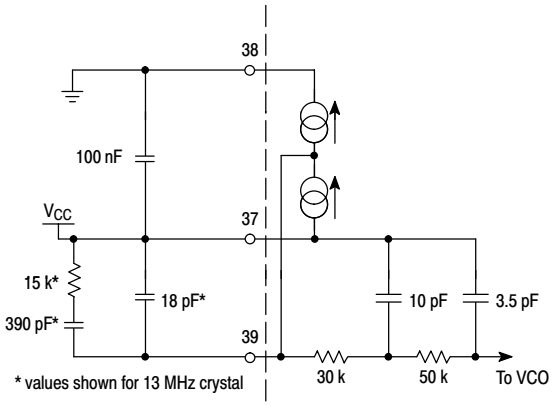
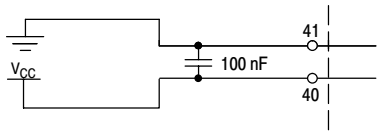
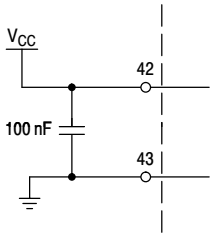
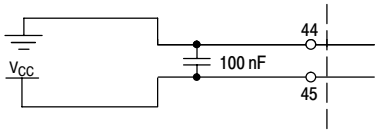
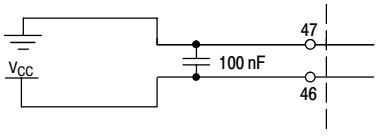
NOTE: VCC = V_{CC}RF

Table 1. Contact Definitions (continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
28	FS		**FS** Frame–sync digital output (used for Rx only). In Receive mode, this signal brackets a 6–bit sample frame.
29	CLK		**CLK** Clock associated with RF data path. Clock Frequency is 24 MHz. Digital output.
30	SCK		**SCK** SPI clock.
31	SDATA		**SDATA** SPI data. Digital input or output.
32	$\overline{CE}$		**$\overline{CE}$** Chip enable is active low enable to facilitate SPI transfers. Digital input.
33	$\overline{RES}$		**$\overline{RES}$** Asynchronous Digital Reset (Active Low). Resets MC13180 register settings to default. Digital Input.

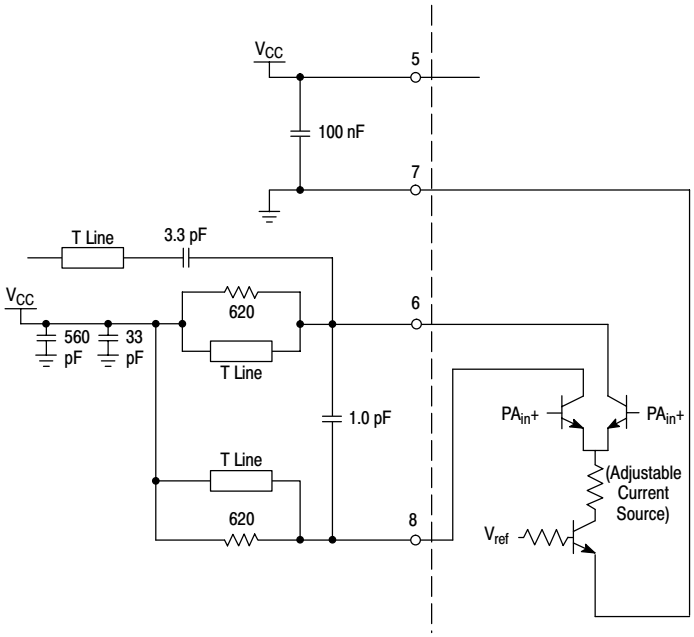
NOTE: VCC = V_{CC}RF

Table 1. Contact Definitions (continued)

Pin	Symbol/ Type	Equivalent Internal Circuit	Description
34	VDDINT		**VDDINT** Digital interface supply voltage. 1.65 V ≤ VDDINT ≤ 3.1 V. VDDINT must, at all times, be ≤ V_{CC}RF.
35	VDD		**VDD** Digital core supply. The pin of the IC is bypassed to gnd. Logic Levels are internally shifted from VDDINT to/from VDD.
36	VSS		**VSS** Digital ground.
38	GNDCP		**GNDCP** Main frac–N charge pump ground.
37	VCCCP		**VCCCP** Main frac–N charge pump V_{CC}. It is decoupled to GNDCP at the pin of the IC.
39	MLPF		**MLPF** Main frac–N loop filter (Charge Pump).
41	GNDPRE		**GNDPRE** Prescaler ground
40	VCCPRE		**VCCPRE** Prescaler V_{CC}. The pin of the IC is bypassed GNDPRE.
42	VCCVCO		**VCCVCO** VCCVCO is decoupled to GNDVCO at the pin of the IC.
43	GNDVCO		**GNDVCO** VCO ground.
44	GNDMOD		**GNDMOD** Modulation DAC ground
45	VCCMOD		**VCCMOD** Modulation DAC V_{CC}. The pin of the IC is bypassed to GNDMOD.
47	GNDMIX		**GNDMIX** Mixer ground
46	VCCMIX		**VCCMIX** Mixer V_{CC}. The pin of the IC is bypassed to GNDMIX.

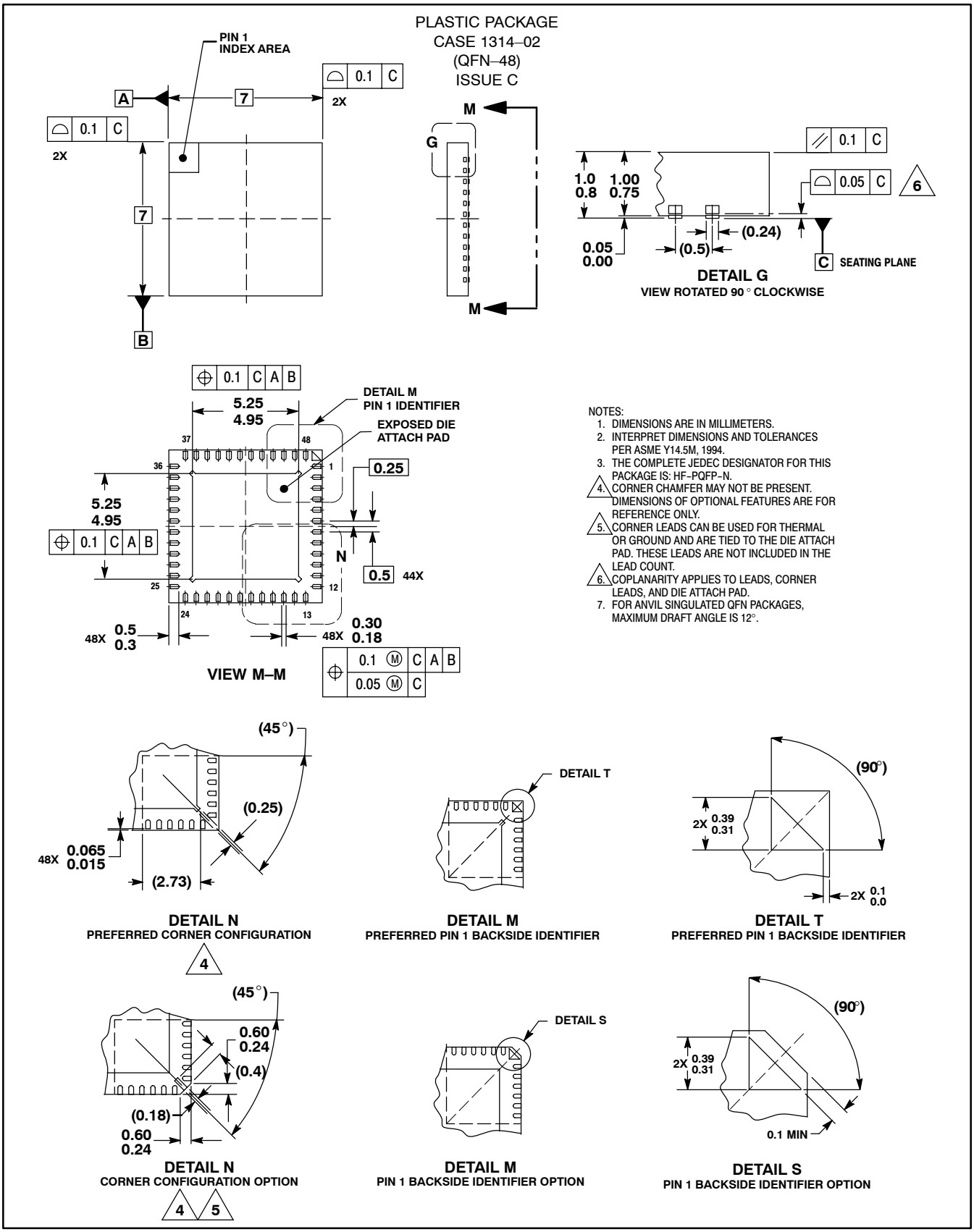
NOTE: VCC = V_{CC}RF

Figure 5. Equivalent Internal Circuit for Pins 5, 6, 7, and 8



3 Packaging

Figure 6. Outline Dimensions



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