Spec Errata
MC68EZ328 User's Manual V1.0

This document covers errata information which relates to the MC68EZ328 (DragonBall EZ) User's Manual version 1.0.

1. External $\overline{\text{DTACK}}$ timing specification.

The "External DTACK Input Setup from CSx Asserted" timing parameters in the following sections are updated.

Section 18.3.2. - Chip-Select Read Cycle Timing (parameter #5).

Section 18.3.3. - Chip-Select Write Cycle Timing (parameter #4)

Section 18.3.4. - Chip-Select Flash Write Cycle Timing (parameter #4)

WAS:

$30 + nT$

NOW:

$30 + (n-1)T$ where n>0 and is the number of wait state in current cycle.

NOTE : Using external DTACK to generate 0 wait state cycles is not recommended.

■■ *SEMICONDUCTOR PRODUCT INFORMATION* ■■

SEMICONDUCTOR PRODUCT INFORMATION